1. OVERVIEW

The VS100 workstation is a 19" monochrome workstation desisned for the professional user. The VS100 consists of a corporate standard multibox containins an H7865 power supply,display processor module,a fiber optics transmitter/receiver module and a bitblit accelerator module. The VS100 uses a 19 in monitor (VR100) in a landscape format. The monitor has a screen resoultion of 1088 pixel horizontally by 864 pixels vertically. The VS100 interfaces to a VAX 11/7XX CPU throush a 10MHz fiber optic cable and a VAX installed Unibus window module. The VS100 is supplied with a LK201Cx keyboard and a VS10X-EA mouse as input devices. An optional disitizins tablet VS10X-BA is available.

2. PRODUCT DESCRIPTION AND FUNCTION

3. PRODUCT REQUIREMENTS

4. STANDARDS,REGULATIONS AND CERTIFICATION

The VS100 complies with the standards and resulations listed in the followins subsections.

4.1 PRODUCT SAFETY

DEC.STD. 119 - disital product safety (covers UL 478, UL 114, CSA 22.2 NO. 154, VDE 0804, and IEC 435)

IEC 435 Safety requirements for data processins equiptment

4.2 AC POWER

DEC.STD. 002 - AC power wirins, sroundins, receptacles and nameplates

DEC.STD. 122 - AC power line standard (operatins frequency 47-63 Hz, operatins voltases 87-128VAC or 174-256VAC).

4.3 ELECTROMAGNETIC COMPATABILITY

DEC. STD. 103 - electromasnetic compability (EMC) hardware desisn requirements.

FCC rules and resulations, part 15 - Radio frequency devices, subpart J (level A)

DIRECTIVE EEC - 76/889-EMI/RFI requirements for the British Isles

VDE 0871 level N-12 - Limits of radio interference from radio frequency apparatus and installations.

4.4 ACOUSTIC NOISE

DIN 45635 PT1 and PT16 - Measurement of airborne noise emmited by machines

VDE 2058 Part 2

DEC.std. 102, section 4 will supercede the above guidelines when available

4.5 ERGONOMICS

ZN1/535 - Ergonomics requirements for display workstations in the office

enviroment.

4.6 ENVIRONMENT

DEC.std. 102 - Environment standard for computers and peripherals (class B, with operating temperature range of 10 to 40 degrees C and 10 to 90 percent relative humidity).

4.7 LANGUAGE

DEC.std. 107 - Digital standard for terminals keyboards

DEC. std. 168 - Multinational character set

4.8 MISCELLANEOUS

DEC.std. 060 - Design and certification of hardware products to national and international regulations and standards.

DEC.std. 092 - Color and finish standard

DEC.std. 105 - Display workstation ergonomics

VDE 0730 - office machine equiptment

VDE 0860 - video display equiptment

4.9 CERTIFICATION AND APPROVAL

The VS100 is designed such that it will obtain the following listings, certifications, and approvals:

(safety) listing against UL 478 and CSA 22.2, No 154

(safety) certification of compliance to IEC 435

(EMI/RFI) international certification of compliance to FCC level A and VDE N-12 level

5. HARDWARE

5.1 DISPLAY PROCESSOR BOARD

5.1.1 DESCRIPTION

The display processor module (DPM) in the VS100 contains the MC68000 cpu,program ram,program rom, screen ram,and I/O ports. Connected to the display processor module as daughter boards are the fiber optic transmitter/reciever (FOT/R) module and the Bit Blit Accelerator (BBA) module.

The timing for the DPM is derived from a 79.96Mhz ECL oscillator and divided down to 40Mhz, 20Mhz, 10Mhz and other lower frequencies for use in the system. The 80Mhz clock allows for a screen display of 1088 pixels horizontally by 864 pixels vertically.

Communication with the host cpu (VAX11/7xx) is thru a fiber optic cable of up to 300 meters in length, which connects to the Unibus Window Module (UBW) located in the VAX unibus backplane. The fiber optic interface operates at a 10Mhz rate. All transmissions across the fiber optic cable are initiated by the DPM's 68000 cpu or by the BBA module. Transmissions to the VAX cpu are 54 bits in length (16 data bits, 16 crc bits, 18 address bits, 1 control bit, 3 spare bits). Recieved data from the VAX cpu is 24 bits in length.(16 data bits, 1 control bit and 7 spare bits). Data is transfered across the fiber link in a BI-PHASE L encoding scheme. All data transmissions are sent with a 16 bit CRC checksum.

The DPM also contains:

a programmable CRTC controller for generating the necessary timing signals for the VR100 monitor

two programmable USART's for communication with the optional digitizing tablet and the LK201Cx keyboard.

A discrete interface for the VS10X-EA hand held mouse

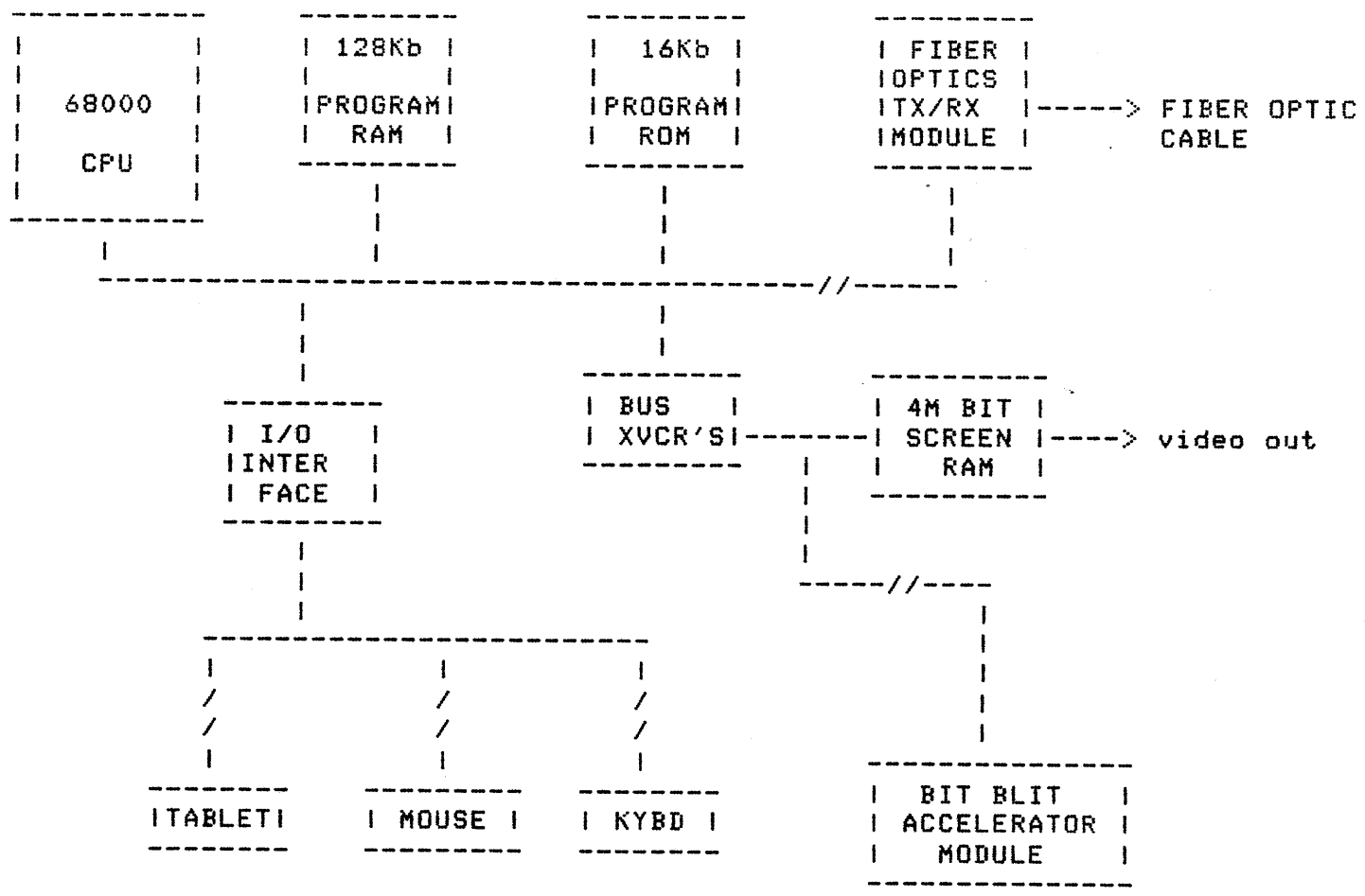
A set of 5 LED's for fault indication. 4 led's are red, and 1 led is green. The led's are located on the rear of the DPM, and are viewable from the rear of the multibox.

A power-up self test diagnostic used for testing of all major portions of the DPM module, the BBA module, the FOT/R module, and the LK201Cx keyboard. An extended set of tests are provided for user tests of the VS10X-EA hand held mouse, the VS10X-BA digitizing tablet, and alignment of the VR100 monitor.

Ilde loop self test that will run continuosly after power-up self test is run, but before the user loss onto the VAX cpu. Idle self-test provide a continuous check of the functionality of the VS100.

The Micro-diagnostics also has a MAINTANCE MODE which will enable the user to run specific tests and to test the I/O devices.

5.1.2. BLOCK DIAGRAM,DISPLAY PROCESSOR BOARD



5.1.3. MEMORY MAP

The VS100 has a total of 656kb on board memory, allocated as follows:

PROGRAM RAM	128Kb
PROGRAM ROM	16Kb
SCREEN RAM	512Kb (4.2M bits)
ADDRESS SPACE	000000-07FFFF = PROGRAM RAM 080000-0FFFFF = UNIBUS 100000-17FFFF = FRAME BUFFER RAM 180000-1FFFFF = PROGRAM ROM

The VS100 can address 256Kb of unibus address space

5.1.4. I/O REGISTERS

The followins devices are mapped into the I/O space (addr 23 = 1) of the MC68000 cpu:

Tablet USART
Keyboard USART
Mouse position register
Crt controller register
System status register
test led register
BBA 'so' f/f

5.1.4.1 CRT controller register

The CRT controller provides the necessary timins signals to the VR100 monitor, and the address for the start of the visible screen memory that will be read out sequentially durins refresh of the screen. The CRT controller has two memory addresses assisned in the I/O space. The first is a pointer register that is loaded with the value of the register that data will be deposited in. Their are 14 registers available for use in the CRT controller.
The second register is the data register. Any data deposited in the data register will be transfered to the register pointed to by the address register.

CTRC ADDRESS REGISTER

address = 8000A0 (HEX) write only

CRTC DATA REGISTER
address = 8000A4 (HEX) read/write

BIT	7	6	5	4	3	2	1	0
	D7	D6	D5	D4	D3	D2	D1	D0

REFER TO DEC. SPEC. A-PS-16963-00 FOR MORE DETAILED INFORMATION

The required parameters for proper operation of the VR100 monitor at a screen resolution of 1088 Horz x 960Vert pixels are:

R0 = 45	R1 = 34
R2 = 37	R3 = 06
R4 = 74	R5 = 05
R6 = 72	R7 = 72
R8 = 00	R9 = 11
R10 = 00	R11 = 00
R12 = 00	R13 = 00
R14 = 00	R15 = 00

5.1.4.2 DISPLAY PROCESSOR STATUS REGISTER

The DISPLAY PROCESSOR STATUS register is used by the MC68000 cpu to obtain the status of events the have an effect on the operation of the VS100 system. This register is a 'read only' register.

address = 8000C0 (HEX) read only

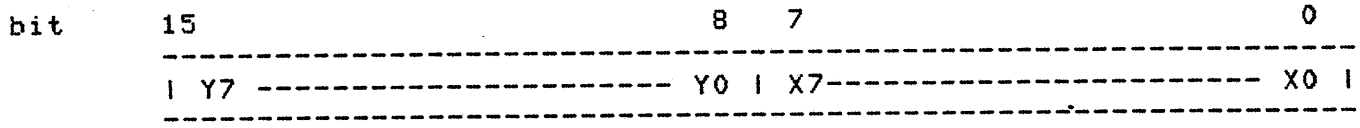
bit	7	6	5	4	3	2	1	0
	D7	D6	D5	D4	D3	D2	D1	XX

bit 7 =	mouse pushbutton,right.	logic 1 (3v) = OFF logic 0 (0v) = ON
bit 6 =	mouse pushbutton,middle.	logic 1 (3v) = OFF logic 0 (0v) = ON
bit 5 =	mouse pushbutton,left	logic 1 (3v) = OFF logic 0 (0v) = ON
bit 4 =	link available	logic 1 (3v) = link is present logic 0 (0v) = link not available
bit 3 =	link error	logic 1 (3v) = link error detected logic 0 (0v) = no link error detected
bit 2 =	non-existant memory	logic 1 (3v) = the UBW attempted to access non-existant VAX memory. Illegable address from the BBA or the DPM. Used as a status bit to indicate the reason for failure to gain access to the UNI-BUS. logic 0 (0v) = address placed on the the uni-bus was a valid address. logic 0 (0v) =
bit 1 =	BBA present	logic 1 (3v) = BBA not present logic 0 (0v) = BBA present
bit 0 =	manufacturing mode	logic 1 (3v) = not in manufacturing mode logic 0 (0v) = the module is in a manufacturing enviroment.

5.1.4.3 MOUSE POSITION REGISTER

The MOUSE POSITION register is used as a count/direction register by the 68000 cpu. This register will contain the value of increments that the mouse was moved since the last 'MOUSE POSITION REG' read by the 68000 cpu.

address = 800060 (HEX) read only



bit 15 = Y7 The M.S.B. of the Y position register. Used to indicate the direction of mouse movement in the vertical axis (Y axis).
logic 1 (3v) =
logic 0 (0v) =

bit 14-8 = the value of the mouse movement in the 'Y' direction

bit 7 = X7 The M.S.B. of the X position register. Used to indicate the direction of mouse movement in the horizontal axis (X axis).
logic 1 (3v) =
logic 0 (0v) =

bit 6-0 = the value of the mouse movement in the 'X' direction.

5.1.4.4 TEST LEDS REGISTER

The TEST LED's resister is used to turn on/off the 4 red led's and 1 sreen led located on the rear of the DPM board. These LED's are used by the micro-diasnostics to indicate failure of any of the major sections of hardware in the VS100 system.

address = 800080 (HEX) WRITE ONLY

BIT	7	6	5	4	3	2	1	0
	XX	XX	OK	G5	R3	R2	R1	R0

bit 7 = RESERVED

bit 6 = RESERVED

bit 5 = TEST OK — Used in the manufacturing enviroment. Indicates that the VS100 has successfully passed burn-in self test. NOTE self test takes approx 20 sec.
logic 1 (3v) = test passed. cleared on power-up, reset by the host, or external init.
logic 0 (0v) = test failed.

bit 4 = sreen led
logic 1 (3v) = led off
logic 0 (0v) = led on indicates the VS100 has passed power-up self test

bit 3 = red led 3
logic 1 (3v) = led off
logic 0 (0v) = led on

bit 2 = red led 2
logic 1 (3v) = led off
logic 0 (0v) = led on

bit 1 = red led 1
logic 1 (3v) = led off
logic 0 (0v) = led on

bit 0 = red led 0
logic 1 (3v) = led off
logic 0 (0v) = led on

REFER TO SECTION 7.5 FOR A COMPLETE DESCRIPTION OF THE TEST LEDS ERROR CODES

5.1.4.5 TABLET USART

The TABLET USART resister is 4 I/O mapped locations used to set-up the 2661 USART for proper communications with the optional VS10X-BA digitizing tablet. The clock to the USART is 5.000Mhz. The normal communications baud rate to the tablet is 9600 baud

address =	800020 (HEX)	READ/WRITE
	800022 (HEX)	READ/WRITE
	800024 (HEX)	READ/WRITE
	800026 (HEX)	READ/WRITE

BIT	7	6	5	4	3	2	1	0
	D7	D6	D5	D4	D3	D2	D1	D0

REFER TO DEC.SPEC. A-PS-18623-00 FOR MORE DETAILED INFORMATION

NOTE: The clock input to the USART is 5.000Mhz

5.1.4.6 KEYBOARD USART

The KEYBOARD USART resister is 4 I/O mapped locations used to set-up the 2661 USART for communications with the LK201Cx keyboard. The clock to the USART is 5.000Mhz. The baud rate for the LK201Cx keyboard is 4800 baud..

address =	800000	READ/WRITE
	800002	READ/WRITE
	800004	READ/WRITE
	800006	READ/WRITE

BIT	7	6	5	4	3	2	1	0
	D7	D6	D5	D4	D3	D2	D1	D0

REFER TO DEC.SPEC. A-PS-18623-00 FOR MORE DETAILED INFORMATION

NOTE: The clock input to the USART is 5.000 Mhz

5.1.5 I/O CONNECTOR DESCRIPTIONS

The following I/O connectors are located on the rear panel of the VS100 DISPLAY PROCESSOR MODULE.

5.1.5.1 MONITOR OUTPUT CONNECTORS

The VR100 monitor uses 3 seperate outputs. These outputs are provided through isolated BNC type 50 ohm connectors. The levels of the outputs are:

video		0.0v-800 mv.
	black =	0.0v
	white =	0.700v
horz.sync		0.4v-2.4v
vert.sync		0.4v-2.4v

5.1.5.2 TABLET POWER AND SIGNAL CONNECTORS

The tablet uses 2 connectors, one for power and one for signals. The connectors are industry standard D-SUB miniature type connectors, located on the backpanel of the DPM module.

9 pin power connector (female, D-sub miniature)

pin 1	+5v
pin 2	+5v
pin 3	N.C.
pin 4	+12v
pin 5	N.C.
pin 6	-12v
pin 7	ground
pin 8	ground
pin 9	chassis ground

25 pin signal connector (female, D-sub miniature)

pin 1	safety ground
pin 2	transmit
pin 3	receive
pin 7	signal ground
pin 12	reserved (test INIT)
pin 13	reserved (test OK)
all other pins =	n.c.

5.1.5.3 MOUSE POWER/SIGNAL CONNECTOR

15 pin power/signal connector (female, D-sub miniature)

pin 1	YA
pin 2	YB
pin 3	XB
pin 4	XA
pin 5	N.C.
pin 6	+5V D.C.
pin 7	N.C.
pin 8	N.C.
pin 9	GROUND
pin 10	GROUND
pin 11	N.C.
pin 12	RIGHT BUTTON
pin 13	MIDDLE BUTTON
pin 14	LEFT BUTTON
pin 15	N.C.

5.1.5.4 KEYBOARD POWER/SIGNAL CONNECTOR

4 pin female telco connector RS-423 COMPATIBLE

pin 1	RECEIVE
pin 2	GROUND
pin 3	+12v dc
pin 4	TRANSMIT

5.1.6 INTERRUPTS

The MC68000 uP on the DPM has 7 levels of interrupt. Level 7, the highest level is non-maskable. Interrupt vector addresses are fixed. The 7 levels of interrupt are:

level 7 = BBA non-existent memory. Set when the BBA tries to address non-existent memory in the VAX cpu. Cleared by clearing the BBA 'so' bit.(the BBA will then clear its memory request, which will clear the LEVEL 7 interrupt.

level 6 = VERTICAL SYNC. used as a watchdog timer. Set by VERT. SYNC. from the CRT controller. Cleared by RESET SIX. (read from address 8000E0 (HEX)

level 5 = LINK TRANSITION. indicates that the Fiber Optic link has had either LINK ERROR asserted, or that LINK AVAILABLE has changed states. Cleared by either a power-up reset (hardware) or a read from address 800040 (HEX)

level 4 = BBA DONE. Used to indicate that the BBA has completed an operation. Cleared by the BBA when the 68000 uP clears the BBA 'go' bit

level 3 = Tablet USART interrupt. Receiver buffer full,or transmitter buffer empty.

level 2 = Keyboard USART interrupt. Receiver buffer full,or transmitter buffer empty.

level 1 = not used

5.1.7 MANUFACTURING MODE

A jumper has been provided on the DPM module that will allow for a dynamic functional burn-in of the zebra/bba/fotr in a manufacturing environment. This jumper requires the use of loopback connectors on the tablet i/o port (DEC. PT# 12-15536-00),and a loopback connector on the keyboard port (DEC.PT# 12-XXXXX-XX). when in this mode,the micro-diagnostics will loop continuously on the power-up self test. The unit will halt at the first occurance of a detected error, and display the test number in the led indicators.

5.2 UNIBUS WINDOW MODULE

5.2.1 FUNCTIONAL DESCRIPTION

The M7452 module is a standard height hex size module used as an interface between the VS100 and the VAX11/7XX cpu. The module connects to the VAX unibus backplane and recieves its power from the VAX. The M7852 is connected to the VS100 by a 2 channel fiber optic cable. The M7452 has 8-16 bit resisters used for the transfer of data between the VS100 and the VAX cpu. The VAX is allowed to address the control/status resisters only. The VS100 can address either the control/status resisters or the VAX memory.

The M7452 is an NPR device and is also capable of interrupts to the VAX. The address range of the module is selected by switches. The interrupt vector addresses are programmable. The Interrupt level is selected by a standard BR chip, set at level BR5.

The unibus module is capable of supporting one (1) VS100 communications link. The maximum length of Fiber optic cable that can used with the VS100 is 300 meters.

5.2.2 MAINTANCE MODE LOOPBACK

The M7452 module is provided with the capability to perform loopback of data while under program control. This is accomplished on two levels. The first is an electrical loopback of data that has been encoded into bi-phase L data at an ECL voltage level. While in this mode, the XMIT ON bit should be dis-asserted. this will prevent data from being transmitted to the VS100 display processor board. Also, while in this mode, the CRC generator may be disabled.

The second level of loopback is the OPTICAL loopback. this mode requires that an optical loopback connector (DEC PT. # 12-yyyyy-zz) be installed on the fiber optic connectors. While in this mode, the XMIT ON bit must be asserted, and the CRC generator may be either asserted or de-asserted.

The loopback process is started by first setting the appropriate bits in CSR 0, then loading the data to be looped back into CSR5. Loading of data into CSR5 will initiate the loopback sequence. Data will be loaded into CSR6. If interrupts are enabled, the unibus module will interrupt the host, with the vector address that was previously loaded onto CSR7.

5.2.3 SWITCH SELECTABLE BUS ADDRESSES

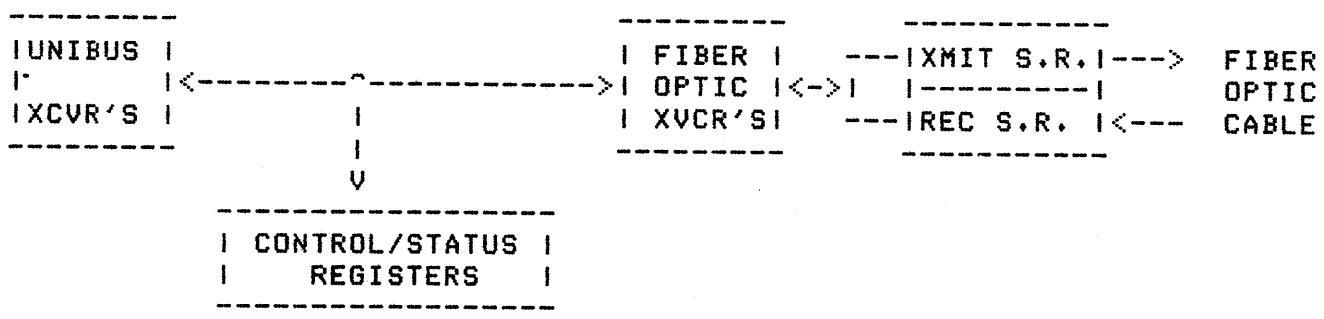
The base address of the M7852 is selectable through a set of switches located on the module. The range of addresses is 760000-777760 (BASE 8) The numbering and location of the switches is as follows:

address bit	12	11	10	9	8	7	6	5	4	UNIBUS ADDRESS
ON	ON	ON	ON	ON		ON	ON		ON	760440(8)
OFF					OFF			OFF		FFE120(16)
switch position	1	2	3	4	5	6	7	8	9	

5.2.4 SOFT VECTOR ADDRESSES

The VECTOR addresses that the VS100 uses to interrupt the host CPU are loaded by the DEVICE DRIVER prior to ucode load. The vector address must be loaded into CSR 7. The allowable range of addresses is 000000-001776(BASE 8)

5.2.4 BLOCK DIAGRAM



5.2.6 CONTROL/STATUS REGISTER BIT ASSINGMENTS

	15	14	13	12	11	10	9	8	7	6	5	4 --- 1	0
CSR 0	LT	LA	LE	XO	MM	CD	MD	RES.	OWN	RES.	IE	FUNCT	GO

BIT 15 Link Transtition
set when:
1. a link error occurs
2. there is a change in the state of the link available bit
cleared by: The host CPU

BIT 14 Link Available indicates the status of the fiber cable squelch circuitry
set when: a sufficient level of light is detected by the fiber optic receiver
cleared by: The host CPU

BIT 13 Link Error
set when: a CRC error is detected by the fiber optic receiver during data reception

cleared by: cleared when the host cpu clears bit 15

BIT 12 Xmitter On used to control the state of the Fiber Optic PIN transmitter diode
set to 1 = light on
cleared to 0 = light off

BIT 11 Maintance Mode controls the state of the U.B.W. module. Allows data to be looped back internally to the module for testing purposes.
set to a 1 = maintance mode enabled
cleared to 0 = normal operation of the module

BIT 10 Crc Disable used by diagnostics to disable the generation of CRC checksums.

set to 1 = disable CRC generation
cleared to 0 = enable CRC generation

BIT 9 Maintance Done used to signal the end of a maintance mode cycle
set to 1 = maintance mode cycle done
cleared to 0 =

BIT 8 RESERVED

BIT 7 OWN

BIT 6 Interrupt Enable

BIT 5 RESERVED

BIT 4-1 FUNCTION CODE specifies an operation to be performed by the display processor.

BIT 0 GO bit

The VS100 micro-code will support the followins 3 functions in ROM based firmware,and the 2 commands associated with the SEND PACKET function.

CODE	BIT POSITION 5	4	3	2	1	FUNCTION
0	0	0	0	0	0	INITIALIZE
1	0	0	0	0	1	SEND PACKET
2	0	0	0	1	0	START DISPLAY

The "SEND PACKET" function has two seperate commands that are supported in the VS100. They are:

1. REPORT STATUS -- this command returns information about the display's status and addressing enviroment to the host.

2. MOVE OBJECT ---- this command allows down-line loadins of the display micro-code into display local memory.

5.3 BIT BLIT ACCELERATOR

5.3.1 FUNCTIONAL DESCRIPTION

The Blit Bit Accelerator (BBA) is used to move data to and from the Display Processor Screen memory at high speed independant of the Display Processor CPU. The BBA recieves command packets from the Display processor, and can modify,manipulate and move data for the purpose of quickly changing visually displayed information.

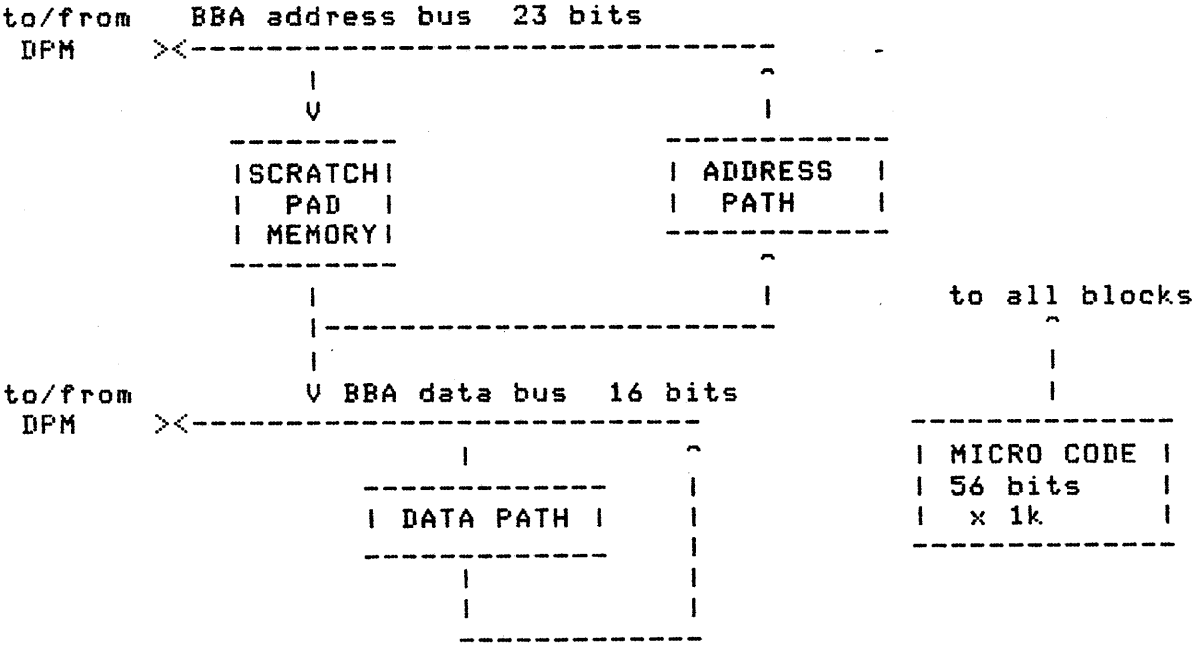
From a functional viewpoint, the BBA is divided into two sections. One secton interpets commands,computes addresses, and provides control and execution of algorithms. The second section is used to process bit data.

The followins instructions are supported by the BBA firmware

A. COPY AREA
B. PRINT TEXT
C. VECTOR
D. HALFTONE

For a complete description of these instructions, refer to the WORKSTATION GRAPHIC ARCHITECTURE V1.0 ,HANK LEVY MARCH 1, 1983

5.3.2 BLOCK DIAGRAM



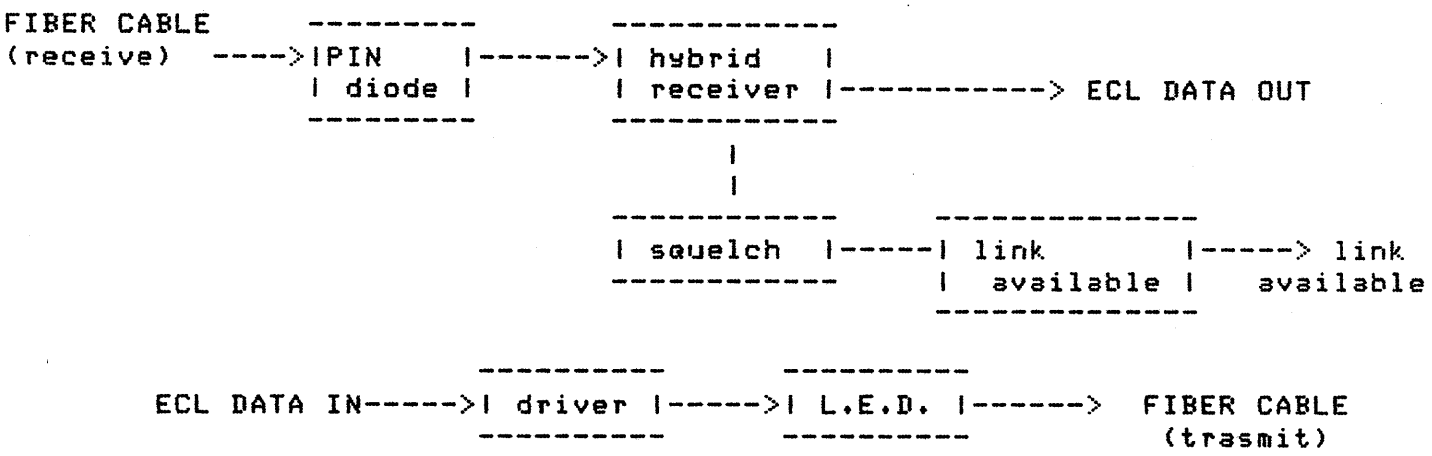
5.4 FIBER OPTIC TRANSMITTER/RECEIVER MODULE (DEC.# 54-16010)

5.4.1 FUNCTIONAL DESCRIPTION

The fiber optic transmitter/receiver module is used to drive the fiber optic cable. The data inputs to the module are ECL level signals, the data outputs from the module are ECL level signals. Also output from the module is the link available signal, used to indicate that the light received is above a minimum value as determined by the squelch circuitry.

NOTE: the link available signal assereted indicates that light is being received. It does not mean that the fiber optic link is functional.

5.4.2 BLOCK DIAGRAM



the FOT/R has four sections. These are: 1. the hybrid receiver, 2. the squelch circuit, 3. the link available circuit and 4. the transmit L.E.D. driver.

5.4.3 SIGNAL DESCRIPTION

40 pin connector, Female

pins 1,2,3,4	+5v
pins 5,6,11,12, 29,30,32,33, 34,36,37,38, 40	GND.
pins 7,8,9,10	+12v
pins 13,14,15,16	-12v
pins 17,18,22, 23,24,25,26, 27,28	N.C.
pin 19	link avail H
pin 20	link avail L
pin 21	xmit on H
pin 31	ecl tx data L
pin 35	ecl tx data H
pin 39	ecl bip data L

5.5 FIBER OPTIC CABLE

DEC.PT# 17-00333-01 unterminated
DEC.PT# 17-00343-xx terminated (BC25B-xx)

The fiber optic cable used in the VS100 is a two channel cable, that operates in a graded-index mode of operation. the optical fiber is 100nm in diameter, clad with glass that is 140nm in diameter.

5.5.1 WEIGHT

The weight of the fiber optic cable is 100 lbs/km nominal, 45kg/km nominial

5.5.2 COLOR

The color of the outer jacket of the cable is TAN (per DEC. 216 , BEIGE)

5.5.3 CABLE LENGHTS

The terminated cable is available in standard lengths of:

DIGITAL PART NO.	DIGITAL OPTION NO.	LENGTH (-0%+2%,+30cm.)
17-00343-02	BN25B15	15M (49 ft.)
17-00343-03	BN25B30	30M (98 ft.)
17-00343-04	BN25B60	60M (197 ft.)
17-00343-05	BN25B90	90M (295 ft)
17-00343-01	BN25B150	150M (492 ft.)
17-00343-06	BN25B300	300M (984 FT.)

The cable is available in the unterminated version only on special order. The DEC pt# for unterminated cable is 17-00333-01. All digital cable that meets these purchase specs will have the transmit cable clearly identified. The recieve cable will also be identified. The cable has the followins charactersitcs:

minimum bend radius, fiber cable with outer sheathins
> 3.0 inches, > 7.6cm

minimum bend radius fiber cable without outher sheathins
> 1.0 inch, > 2.54cm

the cable will withstand a crush force of 400LBS./linear inch

5.6 VR100 monitor

5.6.1 DECSRIPTION

The monitor used with the VS100 is a 19in (diagonal) landscape mode monochrome cathode ray tube(CRT) containing all of the necessary electronics for displaying high resolution alphanumeric/graphic video information. It is AC powered, self contained in a compact plastic enclosure and receives video and synchronizing signals thru a 3 conductor cable from the VS100 multibox.

The monitor is equiped with fault indicating LEDs (normally on) and is intended for mounting on a tilt/swivel base. Other key features of the monitor are:

- rear panel mounted controls for brightness and contrast
- self contained power supply
- OCLI anti-glare screen coating
- noise free operation without a fan
- meets class A FCC radiation levels
- UL approved

5.6.2 VIEWABLE AREA

FORMAT:

The viewable presentation is a rectangular format of square pixels with 1088 pixels across the horizontal dimension and 864 pixels across the vertical dimension.

5.6.3 ACTIVE DISPLAY AREA:

With a solid white screen applied and at a maximum signal level of 40 foot-lamberts, the active display size shall be:

Horizontal	354.3mm +- 1.5mm	13.95in
Vertical	281.4mm +- 1.5mm	11.08in
screen aspect ratio	1.26:1	

5.6.4 PIXEL SIZE:

Horizontal	.325m	0.0128 in
Vertical	.325mm	0.0128 in
pixel aspect ratio	1:1	

5.6.5 FAULT INDICATING L.E.D.S

The VR100 monitor is equiped with 4 fault indicating LEDs. These LEDs are normally illuminated to indicate the presence of the necessary signals/voltages for the proper operation of the monitor.

The LEDs indicate the following conditions:

VIDEO	minimum threshold of 300MV required
HORZ SYNC	TTL level required
VERT SYNC	TTL level required
B+ Voltage	80% of required B+ level for normal operation of the monitor is available

figure of back panel

T.B.S.

5.6.6 POWER REQUIREMENTS

115v @ 1amp. 240v @ .5amp
fuse type = 3AG (U.S.)
5mm X 20mm (EUROPEAN)

5.6.7 CONTROLS,EXTERNAL

brightness
contrast

5.6.8 INPUTS

The inputs to the VR100 monitor are BNC type connectors, located on the rear panel of the monitor.

5.6.8.1 VERTICAL

V. sync width =	0.1 to 0.5 Msec
V. sync period =	16.667 Msec
V. sync. Tr = <3ns.	Tf = <3ns.
V. blanking interval	0.775 Msec
V. unblank interval	15.912 Msec
V. frequency =	60Hz.

5.6.8.2 HORIZONTAL

H. sync width =	2-8 uSEC
H. sync. period =	18.416 uSEC
H. sync. Tr = <3ns.	Tf = <3ns.
H. blanking interval	4.804 uSEC
H. unblank interval	13.612 uSEC
H. frequency =	54.3KHz.

5.6.8.3 VIDEO

Voh =	(white level)
Vol =	(black level)
Tr =	< 3ns.
Tf =	< 3ns.

5.6.9 POWER REQUIREMENTS

120v ac @ 1amp
240 v ac @ .5 amp

5.6.10 PHYSICAL DIMENSIONS

height(w/o tilt/swivel) = 14.75 in. (37.5cm)
width = 18.0 in. (45.7cm)
depth = 16.0 in. (40.6cm)
weight(w/o tilt/swivel) = <45 lb. (20.5 kg)

5.6.11 TILT/SWIVEL BASE

supplied with each unit. customer installed

swivel range = 360 degrees (limited by the cables)
tilt range = -5 to +15 degrees

5.7 MOUSE VS10x-EA

5.7.1 DESCRIPTION

The MOUSE is a hand held pointing device used to select objects on the display screen. It is attached to the display processor module through a 12ft. cable with a male 15 pin D-sub miniture connector. Power for the MOUSE is derived from the display processor module. The MOUSE provides relative position data to the display processor by means of quadurature encode signals for each axis (X and Y). The MOUSE also has 3 buttons used to signal events to the display processor. The mouse buttons are numbered 1 thru 3 from left to right.

5.7.2 PHYSICAL DIMENSIONS

Height = 1.3 in (3.3cm)
Length = 3.75in (9.5cm)
Width = 2.75in (7.0cm)
Weight = <10oz. (280gr.)

cable length = 12 FT.
cable color = DEC 068 GREY

5.7.3 SIGNAL DESCRIPTION

15 pin D-SUB miniature connector type,male
pin 1 thru 15

NOTE: cable shield is tied to the metal housing of the connector.

5.7.4 ACCURACY

The VS10x-EA is capable of providing 200 pulses/inch. The rate of movement of the MOUSE is limited to 10 in/sec.

5.7.5 POWER REQUIREMENTS

+5Vdc +/-10% @ <150ma. protected by a circuit board mounted "pico"fuse.

Note: the "pico" fuse is not customer serviceable.

5.7.6 OPERATION

5.8 TABLET, W/5 BUTTON PUCK DEC. PT. # 30-20037-01

5.8.1 DESCRIPTION

The VS10X-BA digitizing tablet is highly accurate absolute positioning device used to input coordinate data to the display processor board. The digitizing tablet is connected to the display processor by two cables. One is a 9 pin cable used to supply power to the tablet, and the second cable supplies data to and from the tablet. The tablet itself is a micro-processor controlled device, with a hand held puck which has 5 buttons for controlling the operation of the tablet.

The VS10X-BA is a digitizing system consisting of the following components

TABLET	VS10X-CA
5 BUTTON CURSOR	VS10X-DA
12 FT POWER CABLE	17-00341-01
12 FT SIGNAL CABLE	17-00322-06

The digitizing tablet is a computerized input device which sends X-Y coordinate date to the VS100 to indicate the position of the cursor on the surface of the tablet to a high level of accuracy

5.8.2 ACCURACY

The accuracy of the tablet is 1000 Lines/inch at 22 deg.C +/- 4 deg. C at the specified humidity and altitude

REPEATABILITY +/ - 0.001 inch (with cursor)

COORDINATE ORIGIN: absolute

5.8.3 OPERATION OF THE TABLET

The tablet may be operated in any of the following modes of operation

POINT: stylus switch or cursor indicates a single X-Y output

CONTINUOUS: Multiple X-Y pairs are output as long as the stylus or cursor is in the proximity of the tablet. No switch activation is required.

LINE: Multiple X-Y pairs are output as long as the stylus or cursor switch is held down.

INCREMENTAL: Movement of the stylus or cursor of more than 0.01 inch in line mode initiates output.

5.8.4 PHYSICAL DIMENSIONS

5.8.4.1 DIGITIZING TABLET VS10X-CA

height 2.171 in (55mm) in level position
4.203 in (122mm) in tilt position

tilt angle 14 deg +/- 2 deg.

width 16.75 in (425 mm)

depth 16.75 in (425 mm)

weight

5.8.4.2 USEABLE SURFACE SIZE

The surface is seamless, opaque acrylic plastic

width 11.0 in (273.4 mm)

depth 11.0 in (273.4 mm)

5.8.5 POWER REQUIREMENTS

5V DC < 2.0 amp
+12V DC < 120ma
-12V DC < 120ma

5.8.6 SIGNAL DESCRIPTION

I/O cable, 25 pin male, 12ft. (3.7m),DEC 068 grey

pin	function
1	ground
2	transmit data
3	recieve data
4	request to send
5	clear to send
6	data set ready
7	ground
8	carrier detect
20	data terminal ready
other pins	reserved for other functions

POWER CABLE, 9 pin female, 12ft. (3.7m), DEC 068 grey

PIN	FUNCTION
1	+5v
2	+5v
3	N.C.
4	+12v DC
5	N.C.
6	-12v DC
7	ground
8	ground
9	n.c.
shell	chassis ground

5.8.7 RELIABILITY

The M.T.B.F. shall be > 10,000 hrs.

5.8.8 DATA FORMAT

figure to be supplied

5.8.9 SWITCH POSITION SETTINGS

figure to be supplied

5.9 LK201-CA KEYBOARD

5.9.1 DESCRIPTION

The keyboard used with the VS100 workstation is the LK201Cx. This keyboard is a product specific variation of the D.E.C. standard LK201 family of keyboards. For a more detailed description of the LK201 keyboard, refer to the documents listed in the appendix.

5.9.2 MODEL DESIGNATIONS

All LK200 family keyboards are designated by a model number which describes the keyswitch groups implemented, keycap placement,and labeling. The keyboards described here are designated LK201Cx

```
LK201 C x
      - -
      | |
      | ---- alphabetic describing keycap labels.
      |
      ------ alphabetic designating a VS100 specific keyboard.
```

MODEL NO.	KEYBOARD	LEGEND
VS10X-AA	LK201-CA	USA/CANADA
VS10X-AB	LK201-CB	BELGUIM FLEMISH
VS10X-AC	LK201-CC	CANADA (FRENCH)
VS10X-AD	LK201-CD	DENMARK
VS10X-AE	LK201-CE	UNITED KINGDOM
VS10X-AF	LK201-CF	FINLAND
VS10X-AG	LK201-CG	GERMANY
VS10X-AH	LK201-CH	HOLLAND
VS10X-AI	LK201-CI	ITALY
VS10X-AJ	LK201-CJ	JAPAN KATAKANA
VS10X-AK	LK201-CK	SWISS (FRENCH)
VS10X-AL	LK201-CL	SWISS (GERMAN)
VS10X-AM	LK201-CM	SWEDEN
VS10X-AN	LK201-CN	NORWAY
VS10X-AP	LK201-CP	FRANCE
VS10X-AS	LK201-CS	SPAIN
VS10X-AZ	LK201-CZ	AUSTRALIA

5.9.3 DIMENSION

The height from the desktop to the finger contact surface of the home row of keys shall be 30mm. +/-1.0 mm.

The overall dimensions for the keyboard are :

width	21 inches	53.3cm
depth	6.75 inches	17.2cm
height (including keycaps)	2.0 inches	5.1cm

The unsculptured keys are mounted on a curved base which will produce a sculptured keyboard profile with unsculptured keys.

The weight of the keyboard with the interconnecting cable is less than 5.0 lbs 2.3kg

5.9.3.1 COLOR

The function keys located on the top row of keys, the cursor keys and the six keys located directly above the cursors will be a neutral color (DEC 217).The color of the remainder of the keys and the keyboard are grey (DEC 068).

5.9.3.2 REFLECTANCE

The keycaps reflect less than 45% of the incident light.

5.9.3.3 LEGEND

figure to be supplied

5.9.3.4 KEYBOARD INTERCONNECT

The keyboard interconnect cable is 16 ft in length. In an uncoiled condition, the cable is 19 ft. The keyboard cable uses a 4 pin male telephone connector at each end.

5.9.3.5 KEYBOARD OPERATION

The operator uses the keyboard to transmit encoded keying events to a buffer in the workstation. A keying event is transmitted when:

1. any key is newly pressed
2. any of a certain set of keys is depressed
3. certain keys are held down and are generating auto repeatkeying events.

except as allowed above, the release of a key is not an event.

data is transmitted from and recieved by the keyboard at a rate of 4800 baud.

transmitted data is in single byte format for a given key. upon receiving a reset command fron the VS100, the keyboard will perform a power-up self test and then transmit a 4 byte code to the VS100. The 4 bytes transmitted at power-up are defined as follows:

first byte	firmware I.D.
second byte	hardware I.D.
third byte	error code or 0 error code can indicate RAM error,ROM checksum error or key down condition
fourth byte	indicates specific key down if any

The user must identify the keyboard to the VS100 ie. what natural language, german,french etc.,either in the set-up mode or throush escape sequences when switching keycaps or keyboards.

5.9.3.6 N KEY ROLLOVER

The keyboard will transmit the last key down even thoush other keys are not released. This will enable the workstation to exibit the N key rollover feature when:

1. "phantom key" possibilities do not exists.

2. The bell of the keyboard can be programmed for various volume levels

3. The keyclick indicator can be programmed to an ON or OFF condition.

5.10 POWER SUPPLY - H7865

5.10.1 OPERATION

The H7865 power supply is a single ended,switch type, regulated AC-DC converter circuit. It utilizes a uni-directional transformer in a half wave transformer coupled mode. The unit operates at a constant frequency and regulation is achieved by pulse width modulation of the inverter primary current conduction time. Primary energy storage is in the input filter capacitors at approximately 300V DC. Discrete pulses of known current are provided to the UUT primary windings with each triggered period of operation. This current is transformed by the UUT and is available at lower voltage and higher current at the secondary windings of the UUT. By increasing or decreasing the pulse width , the available output voltage is affected correspondingly. Hence, a constant output DC voltage is maintained with varying lines and loads by increasing or decreasing the converter pulse width.

5.10.2 ELECTRICAL SPECIFICATIONS

5.10.2.1 AC INPUT SPECIFICATIONS

5.10.2.2 LINE VOLTAGE

Line voltage input range is selected by an operator accessible switch located near the AC inlet connector. This switch requires a small tool, such as a screwdriver to operate.

5.10.2.2.1 120V AC nominal, single phase, 3 wire.
87V AC to 128V AC.

5.10.2.2.2 220V AC nominal, single phase, 3 wire.
174V AC to 256V AC.

5.10.3 FREQUENCY

5.10.4 CURRENT

5.10.4.1 6A RMS Maximum (87V AC input for full rated output)

5.10.4.2 4A RMS Maximum (174V AC input for full rated output)

5.10.5 POWER FACTOR

The power factor $\frac{\text{RMS WATTS}}{\text{RMS volts x RMS amps}}$ of the input shall be greater than 0.60 at full output power and 120V AC, 60 Hz line.

5.10.6 INRUSH CURRENT

At the first application of input voltage to the power supply, the stated surge current may be reached for 1/2 cycle of the input line. Following that surge, there will be repetitive peaks of exponentially decaying amplitude for up to 10 or more cycles of the line until steady state operation is reached.

128V AC: 70Amps (peak)

256V AC: 70Amps (peak)

5.10.7 OVERLOAD PROTECTION

5.10.7.1 An externally accessible circuit breaker is provided to protect the output wiring. The is rated at 6 Amps,250V AC and covers both input voltage ranges.

5.10.72 The start-up transformer is protected against overheating during a fault by a 1/2 Amp,250V fast blow fuse. This fuse is mounted on the circuit board and is serviceable only by qualified personnel.

5.10.8 REAL INPUT POWER

320 watts input maximum at full rated DC output load.

5.10.9 EFFICIENCY

The ratio of DC output power to real input power at full rated load shall be 0.7 minimum over either input voltage range.

5.10.10 LINE VOLTAGE DISTURBANCE

5.10.10.1 UNDERVOLTAGE

5.10.10.1.1 UNDERVOLTAGE WITHSTAND

The power supply is capable of withstanding any undervoltage condition for any duration without physical damage or degradation.

5.10.10.1.2 RIDE THROUGH

The POK signal(reset to the VS100 mother board) shall remain asserted during one half cycle of less than the minimum line voltage.

5.10.10.1.3 HIGH VOLTAGE TRANSIENTS

NOTE: A spike is defined as a voltage transient, of either polarity and of either common or differential mode, with a rise time (10% to 90 %) of 0.1 microseconds or less and a fall time (to 10%) of 10 microseconds or more.

The average power of spikes shall not exceed 0.5 watts.

5.10.10.1.4 LOW ENERGY TRANSIENTS

The supply shall withstand a 300V peak voltage spike containing not more than 0.2 watt-seconds of energy per spike without sustaining damage or degradation to any portion or component of the supply.

5.10.10.1.5 HIGH ENERGY TRANSIENTS

The supply shall withstand a 1KV peak voltage spike containing not more than 2.5 watt-seconds of energy per spike without sustaining damage or degradation to any portion or component of the supply. This is a one-shot, non-repetitive transient.

5.10.11 ELECTROMAGNETIC INTERFERENCE SUSCEPTABILITY

5.10.11.1 AC POWER LINES

5.10.11.2 CW RF

The power supply shall operate without system degradation with 3 volts RMS superimposed on the AC power interface. (all three lines, power,neutral and ground).

5.10.11.3 TRANSIENTS

The power supply shall operate without degradation when transients with an energy level of 2.5 watt-seconds are superimposed on all conductors (power neutral and ground) of the power cord For testing purposes, the average transient power shall not exceed 0.5 watts.

5.10.11.4 RF FIELD STRENGTH

The power supply shall operate without degradation in the followins fields,100% amplitude modulated with 1000 Hz square wave.

10KHz to 30MHz: 2v/meter
30MHz to 1 GHz: 5v/meter

5.10.11.5 EQUIPTMENT EMINATIONS

In a system confisuration, the interference voltase on all connection to commerical AC power shall not exceed 80 db above 1 microvolt @ 10 KHz, decreasins with frequency to 58 db above 1 microvolt @ 150 KHz-450 KHz and 48 db above 1 microvolt from 450 KHz to 30 MHz. The interference field strensth shall not exceed the followins levels at 30 meters from the equiptment:

Frequency	level	
10 Khz - 30 MHz	50uV/m	(34dbuV/m)
30 MHZ - 1 GHz	17uV/m	(25dbuV/m)

5.10.12 COOLING

Forced air is supplied by a sinsle 12V DC fan. Minimum airflow thru the fan is 27.0 C.F.M., independant of the AC line input voltase.

5.10.13 ACOUSTIC NOISE

At the system level (complete system box with all boards,I/O devices attached and the power supply fan on), the requirements are:

-noise power emmission level < xxxx at zzzzz

-front operator position a-weighted sound pressure

-no promenient tone or impulse noise

meaasurements shall be made and reported in accordance with DEC.STD. 102.4, which includes the requirements of ANSI S1.29, which in turn includes the requirements of ISO 3741 throush 3746 and of ISO 6081 for noise measurements.

5.10.14 ACCESSIBILITY

The power supply case can be opened only by the use of tools.

5.10.15 INPUT/OUTPUT CONNECTORS

5.10.15.1 AC LINE INPUT INTERFACE

AC line input is directly tinto a line filter, thru a three pin IEC connector. An 18AWG power cord is required.

5.10.15.2 AC LINE OUTPUT INTERFACE

A switched AC line output is provided thru a line filter to provide power to the VR100 monitor that is supplied with the system. The switched AC line output has a maximum rating of 1 AMP at 120v AC. Connection to the external device is thru a three pin IEC female connector.

5.10.16 DC OUTPUT CONNECTOR

The followins voltases are available at the power supply output connector.
When viewed from the rear of the power supply,PIN 1 is on the right.

PIN	VOLTAGE
1	DCOK
2	N/C
3	POK
4	-12V dc
5	+12V dc
6	+5V dc
7	+5V dc
8	+5V dc
9	+5V dc
10	GND
11	GND
12	GND
13	GND
14	GND
15	GND
16	GND

5.11 MULTIBOX

5.11.1 The VS100 is housed in a corporate standard multibox

figure to be supplied

5.11.2 PHYSICAL DIMENSIONS

height	=	6.65 in (16.9cm)
width	=	19.21 in (48.9cm)
depth	=	14.31 in (36.4cm)
weight	=	T.B.S.

5.11.3 COLOR

The color of the multibox is DEC 068 grey, with DEC 217 grey trim

6.0 FIRMWARE

6.1 ROM RESIDENT

A. SIZE --- 16k x 16 bits (word)

B. INSTRUCTIONS 3 basic commands
copy area
move object
start display

C. FLOWCHART

T.B.S.

D. OPERATION

T.B.S.

6.2 RAM RESIDENT

A. SIZE

T.B.S.

B. INSTRUCTIONS

T.B.S.

C. FLOWCHART

T.B.S.

D. OPERATION

T.B.S.

7.0 MICRO DIAGNOSTICS

OVERALL MICROCODE STRATEGY

The VS100 microcode is defined as the 16.0 kilobyte powerup/diagnostic package, implemented in Motorola 68000 assembly language, and resides in read-only memory on the Display Processor Module. The microcode is responsible for down-loading the display firmware, but is otherwise invisible to the host. Host (VAX-11) diagnostics are the property of the Macro Diagnostic package, but may call the Micro Diagnostics via the Reset function. When the user logs in, control over the 68000 uP shifts from the microcode to the display firmware.

The microcode is comprised of four major sections; Powerup, Idle Loop, Command Loop and Maintenance Mode. The Powerup code is responsible for testing and initialising all hardware on the terminal end of the VS100 system. The Idle Loop performs a modified continuing sequence of the Powerup code; and polls between tests for Host WGA commands, Mouse Login events, and Keyboard Maintenance Mode entry events. The Command Loop waits for and processes WGA Commands until the host sends the Reset Command to return the processor to the Idle Loop. Maintenance Mode is used primarily to test the four input/output devices that may be attached to the VS100 terminal:

1. DEC LK201 Universal Keyboard
2. Philips Monochrome 19"/60Hz P4 Landscape Monitor
3. Hawley 3-button Mouse Pointing Device
4. GTCO 11" Digi-Pad Graphic Tablet with 5-button Cursor (optional)

These devices require a human interface, although the Keyboard and Table

t

also have self-tests which are called by the Powerup code.

7.0.1 POWERUP SELF-TEST

Tests occur in order of increasing logic complexity, in order to maximise error detection and minimise the chance of a catastrophic system failure. The 68000 remains at priority level seven (all maskable interrupts disabled) until all I/O control chips have been tested and initialised. At this point, the priority level is lowered to zero (all maskable interrupts enabled).

The Powerup code should run less than twenty seconds; the expected cold-start warm-up time for the monitor. The Keyboard's 70-millisecond Self-Test runs in parallel, but is under the control of the Keyboard's central processing unit. At the end of Powerup Self-Test, one of two icons is displayed on an otherwise white screen:

1. Mouse Login Icon -- displayed if there were no Powerup errors.
2. System Failure Icon -- displayed if there were Powerup errors.

In addition, the keyboard's bell is rung when the Mouse Login Icon is displayed, to let the user know that the terminal is ready for normal operation. Logins are disabled if there were errors on Powerup, but are not disabled if errors are found during Idle Loop. Once the user hits a mouse button to login, however, there is the chance that the link may be down or may go down while transmitting the mouse event to the host. In this case, the Mouse Login Icon is replaced by a third icon; the Link Down Icon. Whenever this icon appears on the screen, it is up to the host to reinitiate communication with the terminal.

The Powerup code is structured so that confidence is built hierarchically. Each procedure first checks the error flag, and skips over the diagnostic portion if there were any previous errors (only the first detected error is reported, and further initialisation functions only to enable entrance to Maintenance Mode). Tests are executed in the following order:

A. SIZE contained in the F/W roms appr 6kb

B. OPERATION

on power-up of the system, the u-diagnostics will perform a self test of the mother board, BBA board,FOT/R board,the fiber optic link and the UBW board. The test coverage is >80%. Errors will be reported by means of the leds located on the rear of the mother board, and reported to the host CPU if possible. on successful completion of the power-up tests, the GREEN led on the motherboard will be lit, and the u diagnostics will enter IDLE self test until the user presses a mouse button.

7.0.2 DC POWER SUPPLY

When power is initially applied to the Mother Board, an internal RESET L signal provides a 100ms RESET signal to initialise the hardware to a known state. If the H7862 Power Supply voltages are not within tolerances (DC OK negated), RESET L will be held true; thereby preventing the microcode from starting. The RESET L signal turns all five Mother Board LED's (1 Green, 4 Red) on, which provides a test of the LED's themselves. At the end of RESET L (negated), the Powerup code blinks the LED's off and on again once. This action also causes the state sequencers to remap ROM from $000000 to $180000.

7.0.3 MOTOROLA 68000 MICROPROCESSOR

Two checkerboard test patterns ($55 and $AA) are used, first for byte path immediate data and next for longword path immediate data, using register d0.

Once d0 has been verified for immediate addressing, it is reloaded with the first checkerboard pattern, $55555555. This pattern is then cascaded through all eight data registers (d0-d7) and all seven address registers (a0-a6). The routine is then repeated with d0 initialised to the second checker-board pattern, $AAAAAAAA. This routine validates register RAM space and register source and destination effective addressing modes.

The third step is to test three logical instructions; 'and', 'eor', and 'or'. After that, the signed multiply and divide instructions are verified, and finally the left-shift and right-rotate instructions are verified.

The final step is to test bit manipulation using the BCLR, BSET, and Scc instructions. This is a particularly important step, as the diagnostics rest heavily on the functionality of the bit-oriented instructions to determine their path.

7.0.4 ROM CHECKSUM

The ROM verification routine compares the truncated 8-bit computed checksum against the correct value (stored at the end of ROM). This checksum is computed by a VAX-11 FORTRAN utility, and is inserted into the final byte of the source file before creating the master set of ROM's.

7.0.5 PROGRAM MEMORY

A cursory memory test is performed, using 32-bit longword instructions. The test is in three basic sections:

1. Clear program memory (write all zeroes). This performs an initial check on continuity of memory addressing.
2. Restart at the beginning of memory. Read the current longword for all zeroes, write all ones, read for all ones and progress to the next longword until end of memory.
3. Restart at the beginning of memory. Read the current longword for all ones, write checkerboard pattern #1 ($55555555), read to verify, write checkerboard pattern #2 ($AAAAAAAA), read to verify, clear the location (write all zeroes), read for all zeroes and progress to the next longword until end of memory.

7.0.6 VECTOR INITIALISATION

All 256 exception vectors are initialised to point to exception-recovery code. Unimplemented vectors point to a common exception handler which cleans up the stack and, when in Maintenance Mode, generates an error message indicating which vector occurred and what the value of the access address and program counter was.

7.0.7 MOTOROLA 6845 CRT CONTROLLER

The only read/write register of the CRTC is the cursor register, which we test by writing and immediately verifying all data patterns available; decrementing from $FFFFFF to zero. Upon completion of the diagnostic, registers are initialised to define the screen size as 1088 pixels wide by 864 pixels high (giving a pixel separation of approximately 1/78 inches, or .3256mm); as follows:

R0	(1472/32)-1	= 45	total horizontal characters per line -1
R1	1088/32	= 34	displayed horizontal characters per line
R2	(1088/32)+3	= 37	horizontal sync position in characters
R3	(0*16)+6	= 06	vertical/horizontal sync widths in characters
R4	(900/12)-1	= 74	total vertical character rows per screen -1
R5	5	= 05	adjustment to vertical sync to force 60-Hz
R6	864/12	= 72	displayed vertical character rows per screen
R7	(864/12)+1-1	= 72	vertical sync position in character rows +1 -1
R8	0	= 00	non-interlaced mode, no skew
R9	12-1	= 11	scan lines per character row -1
R10	0	= 00	cursor start
R11	0	= 00	cursor end
R12	0	= 00	start address high byte
R13	0	= 00	start address low byte
R14	0	= 00	cursor high byte
R15	0	= 00	cursor low byte

7.0.8 TABLET PORT

Internal loop-back mode is set on the Tablet USART, and the same scheme used to test the CRTC Cursor Register is implemented here on the data holding register. The internal loop-back scheme requires that the mode registers be set up for normal operations, in order to test the USART as it would normally be used. Therefore, the Tablet USART is initialised preceding the test, as follows:

```
Baud Rate <-- 9600
Parity Control Disabled
Asynchronous Receive/Transmit Mode
1 Stop Bit
8 Data Bits (Character Length)
I/O <-- 16 x Baud Rate
```

The I/O bit is initialised to 16 times the Baud Rate factor to account for byte-length characters. Following the test, the receiver is enabled and the transmitter disabled. The transmitter must be enabled prior to each transmit operation, as transmit interrupts are cleared by disabling the transmitter.

7.0.9 KEYBOARD PORT

Internal loop-back mode is set on the Keyboard USART, and the same scheme used to test the CRTC Cursor Registers is implemented here on the data holding register. The internal loop-back scheme requires that the mode registers be set up for normal operations, in order to test the USART as it would normally be used. Therefore, the Keyboard USART is initialised preceding the test, as follows:

```
Baud Rate <-- 4800
Parity Control Disabled
Asynchronous Receive/Transmit Mode
1 Stop Bit
8 Data Bits (Character Length)
I/O <-- 16 x Baud Rate
```

The I/O bit is initialised to 16 times the Baud Rate factor to account for byte-length characters. Following the test, the receiver is enabled and the transmitter disabled. The transmitter must be enabled prior to each transmit operation, as transmit interrupts are cleared by disabling the transmitter.

7.0.10 FIBRE OPTICS ELECTRICAL LOOP-BACK

The Fibre Control Resister is set for Electrical Loop-Back Mode, and two checkerboard patterns ($5555 and $AAAA) are then written to the Host Control and Status Resister individually. After writing each pattern, NXM is checked for error status on the packet. If NXM is okay, then the pattern is read back from the loop-back address. If the packet returns bad information, the data will be either all ones or all zeroes. Following this test, the Fibre Control Resister is set for Powerup State and Link_Available is checked. If the host's fibre light is on, the Link_Available software flag is set and the terminal's fibre light is set at the end of Powerup (provided that a Link Transition interrupt is not received in the meantime). Otherwise, the terminal's fibre light remains off until a Link Transition interrupt occurs. Any time the Fibre Control Resister is written to, it must be followed by a 1ms timer to allow the host time to receive the new status.

7.0.11 VSYNC VECTOR TIMEOUT

Interrupt are now enabled. If we do not receive a vsync interrupt within 100ms, a failure is reported.

7.0.12 FRAME BUFFER MEMORY

The same scheme is used as in the Program Memory test; though frame buffer memory is tested in four quadrants, for the sake of speed and modularity. Each quadrant of frame buffer memory is the same size as program memory, so the frame buffer test entails four calls to the common memory test.

7.0.13 BIT-BLOCK TRANSFER ACCELERATOR MODULE

The VS100 status resister is checked for the presence of the BBA. If the BBA is present, four tests are executed:

1. Scratchpad RAM -- all 256 words
2. Copyarea
3. Halftones
4. Vectors

7.0.14 KEYBOARD SELF-TEST

A request for the keyboard's hardware ID times out after 1 second. If the ID is received, we then call the keyboard's self-test. It is necessary to call the Self-Test again at this point, as the results the previous Self-Test could not be interpreted by the uninitialised 68000. The results of the current test are reported to the Keyboard LED's, and to the 68000 via the following four-byte message:

BYTE 1: KBID (Firmware) -- The Keyboard ID which is stored in firmware
BYTE 2: KBID (Hardware) -- The Keyboard ID which is read from Jumpers in the hardware
BYTE 3: ERROR CODE (Self-Test)
  00 No Errors
  3D Key down on Powerup
  3E Self-Test Failure, ROM or RAM
BYTE 4: KEYCODE (Powerup)
  00 No keys down on Powerup
  xx Code for first key down on Powerup

If the keyboard does not respond with the hardware ID after one second, an error is assumed and reported.

7.1 IDLE LOOP

After successful completion of the Powerup code, the 68000 continuously loops on a modified version of the same code until the user either logs in or enters Maintenance Mode. If Idle Loop fails a test, it does not do any more testing until the next pass. All errors are logged to the host, but only the first error detected is reported to the Mother Board and Keyboard LED's. The following tests are executed during Idle Self-Test:

1. 68000 CPU (extended)
2. ROM Checksum
3. Program Memory (truncated)
4. Vsync Vector Time-Out
5. Frame Buffer Memory (truncated)
6. BBA Scratchpad Memory
7. Keyboard ID

Between tests, Idle Loop polls for mouse buttons (in which case the host is informed), host commands (in which case we branch to the command loop), and control/shift/f4 (in which case we branch to maintenance mode). After a mouse button is hit, we initialise a counter and increment it during vsync for five seconds. Between tests, we check this flag to make sure the five minuts are not up. If we have not received a command from the host in that time, and link is available, we can assume the host is dead in the water and put the Link Down icon up on the screen.

7.2 COMMAND LOOP

The host may request the VS100 to perform WGA commands at this point. The following commands are defined at microcode level:

1. Reset (go to Idle Loop via Powerup diagnostics)
2. Send_Command_Packet (includes Move_Object and Report_Status Commands)
3. Start_Display_Firmware (transfers control to the display firmware)
4. Init (initialise CSR's and go to command loop)

Init initialises the Control/Status Registers as follows:

1.	CSR #0 (Control/Status Register)	Untouched; taboo!
2.	CSR #1 (Interrupt Reason Register)	Bit 1 <-- Init_Done
3.	CSR #2 (Peripheral Event Register)	Cleared
4.	CSR #3 (Function Parameter Low)	Unibus_Ram base address low
5.	CSR #4 (Function Parameter High)	Unibus_Ram base address high
7.	CSR #5 (Identification Register)	Bits 3-5 <-- hardware ID
6.	CSR #6 (Unused Register)	Cleared
8.	CSR #7 (Interrupt Vector Register)	Untouched; taboo!

CSR's #5/6 are the X and Y Mouse/Tablet Cursor Position Registers once the display firmware has been downloaded. Refer to the Workstation Graphics Architecture document for details on the Control/Status Registers.

After the first command, we wait in a loop for five seconds for another command. If we do not receive another command in that time, we assume the host is dead in the water, put up the Link Down icon, and exit the command loop to re-enter Idle Loop.

7.3 MAINTENANCE MODE

Several tests are available to test the input/output devices, as well as a special test for the fibre link. All tests in Maintenance Mode require a human interface. This mode is entered by typing <control/shift/f4> while in Idle Loop, and results in the following menu being printed to the screen:

***** VS100 Maintenance Mode -- type function key f4 to exit

Keypad Options:

0 Jump to Powerup
1 Keyboard Test
2 Mouse Test
3 Monitor Test
4 Tablet Test
5 Optical Loop-Back

Typing 'f4' exits the menu and returns to the Idle Loop.

7.3.1 KEYBOARD FUNCTIONALITY TEST

Upon entering the Keyboard Test, the following message is printed to the screen:

***** VS100 Maintenance Mode -- type function key f4 to exit

Keypad Options:

0 Return to Main Menu
1 Keyboard ID Test
2 Keyboard Self-Test
3 Keyboard Loop-Back
4 Keyboard Button Test

If any of the tests is called and fails, the status is printed beneath the menu. The user is advised to execute tests 1-3 (which indirectly tests those keys), then type '4' to select the Button Test. A 'Current Keycode: ' prompt will then appear beneath the menu. Type each of the other keys on the keyboard EXCEPT for the '0' on the keypad. Then 'metronome' any key, and type '0' to exit and return to the main menu. The keycode for the key pressed will be sent to the screen in decimal format, by the 'Current Keycode: ' header. Metronome also results in a code being displayed, as does the release of the shift or control keys. The keyboard button test sits in a loop that polls for keyboard keycodes.

7.3.2 MOUSE FUNCTIONALITY TEST

Upon entering this mode, the following message is printed to the screen:

***** VS100 Maintenance Mode -- type function key f4 to exit

Keypad Options:

0 Return to Main Menu
1 Mouse Button Test
2 Mouse Cursor Test

There are basically two aspects of the mouse that need to be tested; directional/magnitudinal accuracy of the cursor, and communication of mouse button events. If the Button Test is selected, a "Current Button: " prompt appears beneath the menu and records the number of the button that is currently being held down. If no button is depressed, the line contains information on the last button it received. The button test essentially sits on a loop that polls the VS100 status register for mouse buttons.

If the Cursor Test is selected, the screen is erased and a 64 x 64 pixel crosshair cursor is masked to the screen. The cursor is updated at every frame interrupt to indicate movement of the mouse, and is initialised to the screen centre. A 64 x 64 pixel black peripheral box is masked to each of the four corners of the screen at an offset of 64 pixels in each direction (to allow passage of the crosshair cursor around the boxes), against the standard graphics halftone background (halftone #9). The mouse is used to move the cursor onto, around, and inside each of the boxes; to test general directional and magnitudinal correctness.

7.3.3 MONITOR TEST

Upon entering this test, the following menu is printed to the screen:

***** VS100 Maintenance Mode -- type function key f4 to exit

Keypad Options:

0 Return to Main Menu
1 Universal Alignment Pattern
2 Stairstep of Halftones
3 Toggle Screen Contents

For any pattern, the screen is preserved until '0' is hit to exit.

7.3.3.1 TEST PATTERN #1 (Universal Alignment Pattern)

The first monitor test pattern produces a stationary diagram on the screen for adjustments and measurements, in five stages:

1. Periphery Diagram: The first and last pixel of each row and column are lit in order to define the active display area for centring adjustments.
2. Crosshatch Pattern: Centred at a vertical indentation of 42 pixels (13.68mm), and a horizontal indentation of 48 pixels (14.33mm), is a black-on-white crosshatch pattern, comprised of one-pixel wide lines at 1/20 pixel spacing (6.513mm).
3. White Central Outer Box: A white rectangular box of dimensions 608 pixels high (198.01mm) by 448 pixels high (145.89mm) is centred at the screen centre. The box is solid, and is written directly to the screen rather than masked onto the crosshatch. It is only a few pixels shy of being tangent to the white peripheral circle.
4. Black Central Inner Box: A black square box of dimension 112 pixels (36.47mm) is centred at the screen centre. The box is solid, and is written directly to the screen rather than masked onto the white box.
5. Centred Pehripheral Circle: A white circle is generated about the screen centre utilsing Michener's adaptation of Bresenham's circle algorithm. The diameter is 768 pixels (250.1mm), so that the circle is only five pixels shy of being tangent to the crosshatch periphery.

7.3.3.2 TEST PATTERN #2 (Stairstep of Halftones)

The second monitor test pattern is a stairstep of 17 halftones, going from left to right. The first halftone is black, the last halftone is white, and the fifteen halftones in between are the standard VS100 halftones. Each halftone pattern spans the screen height and is 64 pixels wide.

7.3.3.3 TEST PATTERN #3 (Toggle Screen Contents)

Regardless of which test was executed previously, this command toggles the entire current screen contents. This effectively doubles the number of screen patterns available. The pattern can always

be toggled back to what it was by selecting this command again.

7.3.4 TABLET FUNCTIONALITY TEST

Upon entering this mode, the following message is printed to the screen:

***** VS100 Maintenance Mode -- type function key f4 to exit

Keypad Options:

0 Return to Main Menu
1 Tablet Button Test
2 Tablet Puck Test

Similar to the Mouse Test, except that the Tablet has 5 buttons numbered 0-4. For future adaptability to 16-button pucks, a decimal conversion routine is used to report the button number.

7.3.5 FIBRE OPTICS OPTICAL LOOP-BACK TEST

Same as electrical loop-back test in powerup, except the test is performed with the fibre light on, and a loop-back is required.

7.4.0 EXCEPTIONS & INTERRUPTS

All two-hundred fifty-six 68000 interrupts and exceptions are supported by the microcode, whether or not they can be expected to occur. The 68000 provides two kinds of interrupts; Auto-Vectored and Device-Vectored. The VS100 utilises the Auto-Vector system. All unimplemented interrupts and exceptions result in the generation of an error code/message.

7.4.1 EXCEPTIONS

Bus_Errors are generated by accessing non-existant Unibus memory (if NXM is set), when the link goes down while accessing legitimate Unibus memory (not including CSR's, which are always considered to be accessible), or when the retry counter overflows. Address_Errors occur when a word or long-word operand is accessed at an odd address.

Other exceptions are initialised even though unused, in order to insure against hardware/firmware/microcode bugs. All exceptions other than bus errors are recovered from by use of the rte instruction.

7.4.2 AUTO-VECTOR INTERRUPTS

Seven levels of interrupts are available on the 68000, in increasing level of priority. The highest level of interrupt is non-maskable. The auto-vectors are assigned as follows:

Level	Address(hex)	VS100 Device
0	----------	No Interrupt
1	64	Mouse Cursor
2	68	Keyboard Receive/Transmit
3	6C	Tablet
4	70	BBA Command Done
5	74	Link_Transition or Link_Error
6	78	Vertical Sync
7	7C	BBA Non-Existent UBW Memory Access

Keyboard and Tablet Interrupts occur under two conditions: When the USART Holding Register receives a byte of information from the device, a receiver interrupt is generated. When the USART Holding Register transmits a byte of information to the device, a transmitter interrupt is generated. Receiver interrupts are cleared by reading the data from the Holding Register. Transmitter interrupts are cleared by disabling the transmitter.

Vertical Sync interrupts occur at every vertical sync; that is, every 1/60 second. Mouse Buttons are polled during vertical sync handling, for the purpose of reporting login events to the host. Vertical Sync interrupts are cleared by performing a read operation on address $8000E1.

Mouse interrupts occur every time the mouse is moved. The information is stored and used during vertical sync handling to update the mouse cursor when it is attached. Mouse interrupts are cleared by reading data from the mouse cursor.

Link_Error Interrupts are ignored, but Link_Transition Interrupts are used to determine whether or not to turn on the fibre's LED driver at the VS100 end of the system. We store the information of the current state in memory, and examine Link_Available to determine whether to turn the LED on or off. Link_Transition occurs when the state of the LED driver at the UBW end of the system changes.

Each interrupts sets a flag indicating that it occurred. (e.g., level5 sets the "link_transition" flag). These flags are all cleared on powerup.

7.5 ERROR REPORTING

All diagnostics at all levels of microcode attempt to report errors in each of three ways:

1. Error code to Mother Board LED's
2. Error code to LK201 Keyboard LED's
3. Error code to Host's Interrupt Reason Register (CSR #1)

The error code is a nybble (4 bits) code identifying the test that failed. The code is the same for all three error code output forms.

POWERUP: green led off, test # in LEDS. Code set in advance of test. If error, skip rest of powerup diagnostics and freeze the led code during idle loop tests.

IDLE LOOP: green led on, test # in LEDS. Code set in advance of test. If error, replace led code with powerup error code; that is, green led off and test # in leds. Ignore rest of idle loop, freeze leds, but start testing again at beginning of next idle loop.

MANUFACTURING: read status for jumper. Green led on, test # in leds. No keyboard leds or reporting to host or screen message (that is, loop before reaching "process_errors"). Loop on any test that fails, but otherwise loop back to the beginning of powerup (after first locking out interrupt and reloading the stack).

LED Number				Diagnostic Reason
3	2	1	0	
0	0	0	1	68000 CPU error
0	0	1	0	ROM Checksum error
0	0	1	1	Program RAM error
0	1	0	0	CRTC Register error
0	1	0	1	Tablet Port error
0	1	1	0	Keyboard Port error
0	1	1	1	Fibre Optics Loop-Back error
1	0	0	0	Vsync Time-Out error
1	0	0	1	Frame Buffer error
1	0	1	0	BBA Scratchpad error
1	0	1	1	BBA Command error
1	1	0	0	Tablet ID error
1	1	0	1	Tablet Self-Test error
1	1	1	0	Keyboard ID error
1	1	1	1	Keyboard Self-Test error

"0" is used to indicate that the LED is turned off; "1" is used to indicate that it is on. The same code is used for the Keyboard LEDS, Mother Board LEDS and Host Interrupt Reason Register (with bits 14 and 15 turned on to indicate a diagnostic failure). The Mother Board also has a green LED, which is used to indicate the mode that the machine is operating under. During Powerup, the error code on the Mother Board is set in advance of each test with the green LED turned off to indicate that the test failed (in case it does not reach completion). Once the Powerup confidence test is done and we enter Idle Loop, the error code on the Mother Board is set in advance of each test with the green LED turned on to indicate no errors. If the test finds a failure, it replaces the same error code with the Powerup error code; i.e., the green LED is turned off to indicate an error condition. Only the first error detected is reported to the Mother Board LEDS. Once an error is detected, it is reported to the Keyboard LEDS and the Host Interrupt Reason Register. Only the first error detected is reported to the Keyboard LEDS, but all errors are reported to the Host (including bit #4 set to indicate error during Idle Loop versus Powerup failure).

7.6 MANUFACTURING MODE

Manufacturing Mode is entered upon powerup when a jumper is in place next to the Mother Board LED's. In this mode, loop-back connectors are used at the keyboard and tablet ports for special tests that are available ONLY when the jumper is in place and are executed in place of the normal I/O self-tests. At the end of the Powerup Self-Test, the microcode jumps back to a location in ROM (to be determined) and executes the entire self-test. This cycle continues indefinitely.

Manufacturing Mode is a special mode used by the module manufacturing facility during burn-in of the VS100 Mother Board. A jumper has been provided which the 68000 reads to determine whether the module is in a manufacturing environment. When the jumper is in place, the normal Powerup sequence is slightly modified, and error reporting is limited solely to the Mother Board LED's. For Manufacturing Mode to function properly, the following loop-back connectors must be in place BEFORE power is applied:

Tablet I/O	Pin 2 connected to Pin 3
Keyboard I/O	Pin 2 connected to Pin 3
Fibre Optics Optical Loop-Back Connector in Place	

The Bit Block Transfer Accelerator Module is optional: The micro-diagnostic checks for presence of the module, and skips the BBA self-test if the module is not present.

The following tests are modified as follows:

1. Fibre Optics Loop-Back Test
   The electrical loop-back test is now followed by an optical loop-back test, which is the same except for that it requires a special jumper to be in place.

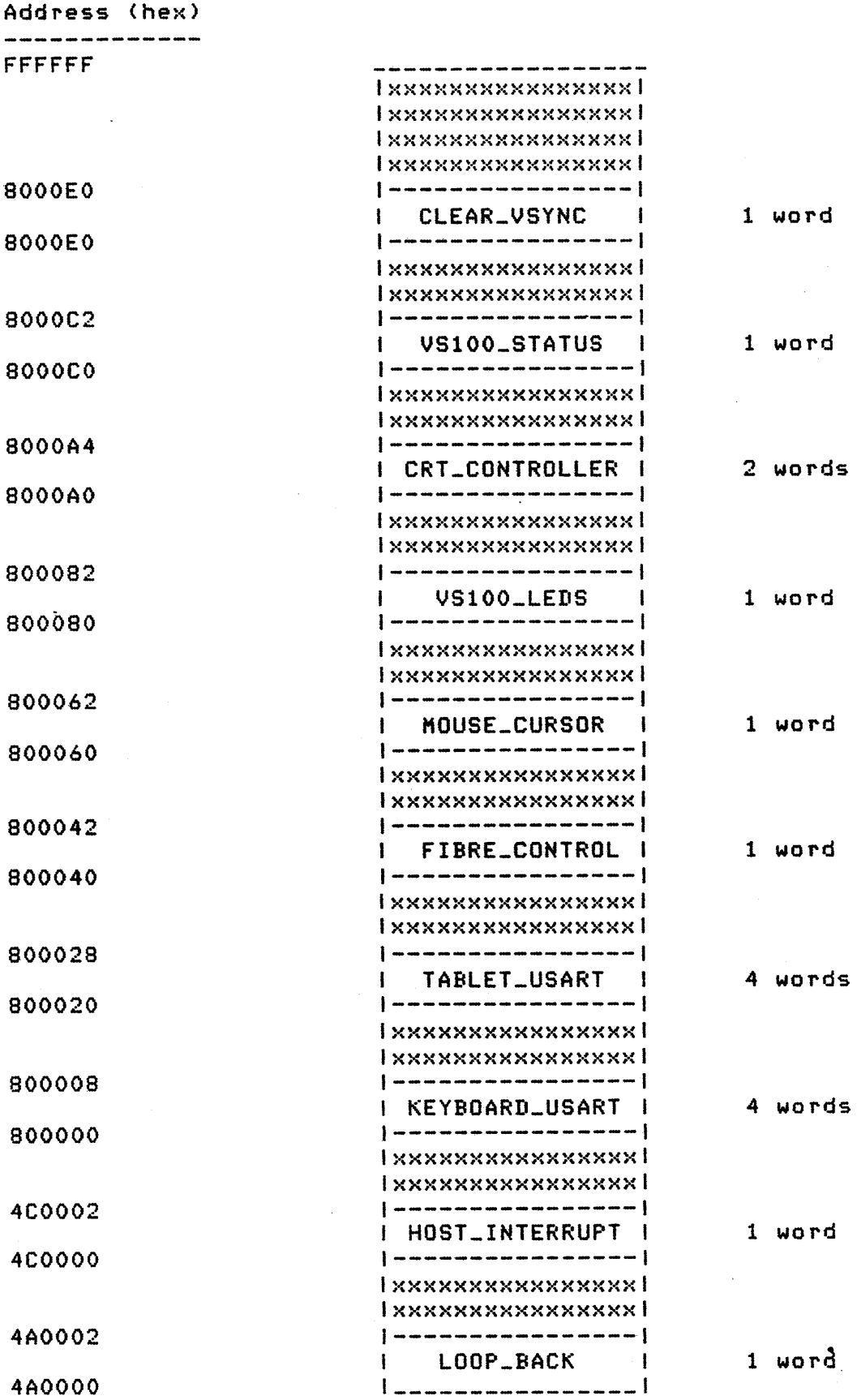
2. Tablet USART Test
   The internal loop-back test is now followed by an external loop-back test, which is the same except for that it requires a special jumper to be in place.

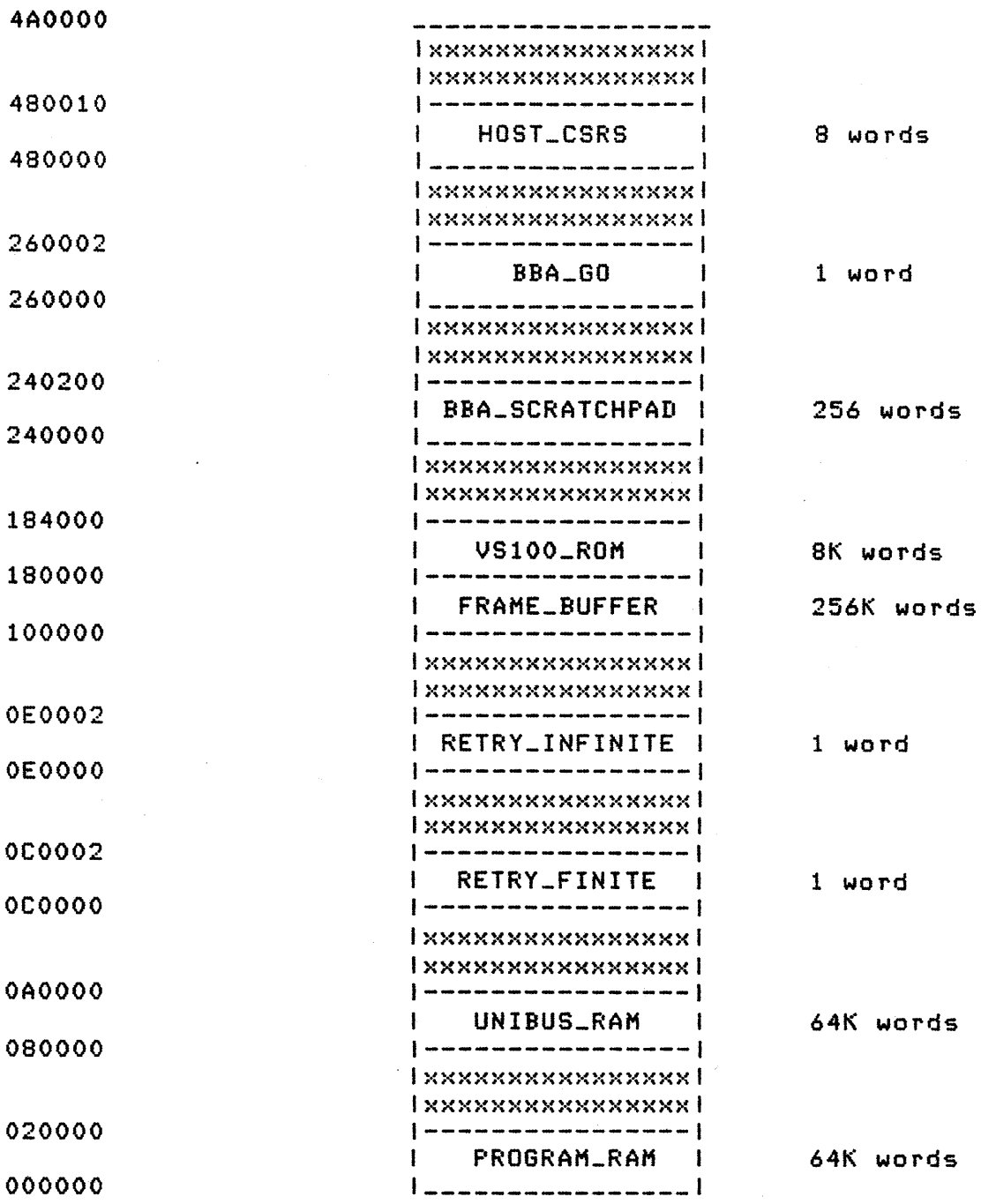
3. Keyboard USART Test
   The internal loop-back test is now followed by an external loop-back test, which is the same except for that it requires a special jumper to be in place.

The following tests are deleted:

1. Keyboard ID Test
2. Keyboard Self-Test

7.7 MC68000 MEMORY MAP




4A0000
480010
HOST_CSRS
8 words
480000
260002
BBA_GO
1 word
260000
240200
BBA_SCRATCHPAD
256 words
240000
184000
VS100_ROM
8K words
180000
FRAME_BUFFER
256K words
100000
0E0002
RETRY_INFINITE
1 word
0E0000
0C0002
RETRY_FINITE
1 word
0C0000
0A0000
UNIBUS_RAM
64K words
080000
020000
PROGRAM_RAM
64K words
000000

7.8 VS100 STATUS REGISTER

Here is a map of the VS100 read-only status register:

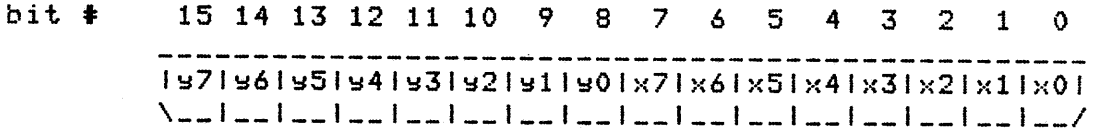
```
bit #  7 6 5 4 3 2 1 0
       | | | | | | | `----- Manufacturing Mode (0 = yes, 1 = no)
       | | | | | | `------ BBA Present (0 = yes, 1 = no)
       | | | | | `------- NXM (0 = no, 1 = yes)
       | | | | `-------- Retry_Overflow (0 = no, 1 = yes)
       | | | `--------- Link_Available (0 = no, 1 = yes)
       | | `---------- Left Mouse Button (0 = yes, 1 = no)
       | `----------- Centre Mouse Button (0 = yes, 1 = no)
       `------------ Right Mouse Button (0 = yes, 1 = no)
```

Manufacturing Mode is set when the host is performing an electrical loop-back on the fibre link at its own end. NXM is set when non-existant UBW memory is accessed from the 68000. If non-existant UBW memory is accessed from the BBA, a level7 interrupt is generated instead. The 68000 generates a bus error when NXM is set, and it is the duty of the microcode to examine this register in the bus error routine to determine the nature of the bus error.

Mouse buttons generate a zero code when depressed, but their status bits otherwise remain high. Link_Available True means that the LED is lit at the UBW end of the fibre link.

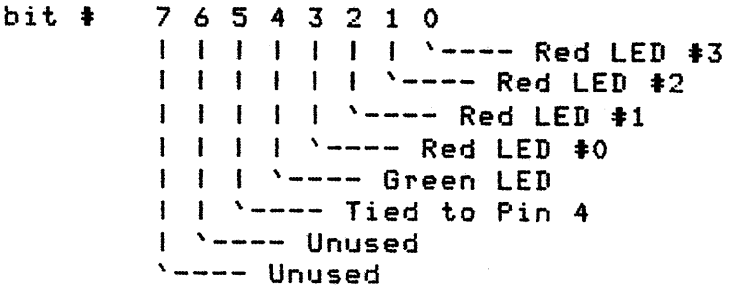
7.8.1 MOUSE CURSOR

The mouse cursor resister contains two eight-bit counters which keep track of the mouse's horizontal and vertical movement:



7.8.2 MOTHER BOARD LED's

There are five LED's on the Mother Board; four red LED's and one green LED. The green LED is used to indicate OK status of the VS100, and the red LED's are used to report error conditions.



7.8.3 FIBRE CONTROL

The fibre control register uses three bits. These are write-only signals, and are used by the hardware. XMIT ON causes the hardware to light the LED at the Mother Board end of the fibre link. The other two signals are diagnostic signals.

```
bit #   7 6 5 4 3 2 1 0
        | | | | | | | `---- Xmit On (0 = no, 1 = yes)
        | | | | | | `----- Maintenance Mode (0 = no, 1 = yes)
        | | | | | `----- Force CRC Error (0 = no, 1 = yes)
        | | | | `----- Unused
        | | | `----- Unused
        | | `----- Unused
        | `----- Unused
        `----- Unused
```

The following bit patterns are defined:

Xmit On	Maintenance Mode	Purpose
0	0	Powerup State
0	1	Electrical Loop-Back
1	0	Normal Operation
1	1	Optical Loop-Back

7.8.4 USART's (Motorola 2661 EPCI's)

Each USART has four registers that are accessible by the 68000. The map is as follows:

Byte 1 Holding Register
Byte 3 Status Register
Byte 5 Mode Registers
Byte 7 Control Register

The first time one writes to Byte 5, one accesses Mode Register 0. Thereafter, any reference to Byte 5 refers to Mode Register 1. Byte 1 refers to the Transmit Holding Register or the Receive Holding Register, depending on whether one is performing a read or write operation.

7.8.5 CRT CONTROLLER

The CRT Controller is two bytes. Byte 1 is the address pointer. Byte 2 is the data register. You must write the value of the register you wish to write to into the address pointer before writing the desired value of that register into the CRTC's data register.

8.0 SOFTWARE

1. OVERVIEW WGA/SDA
2. DESCRIPTION
3. OPERATION
4. DEVICE DRIVER

The device driver for the VAXSTATION 100 display will permit a callins program to send command and argument lists to the VS100 DISPLAY PROCESSOR. In addition to this basic function, the driver can be instructed to start and stop the display processor,load the processor microcode from VAX memory or disk, and load character fonts.

9.0 PERFORMANCE

1. HARDWARE LIMITS
    A. memory access cycle time = 400ns.
    B. screen memory access time = 800ns.
    C. unibus memory access time =
        1. fiber optic
        2. worst case unibus access time
        3. vax memory cycle time

2. SOFTWARE OVERHEAD

    T.B.D.

10.0 MAINTAINABILITY

RELIABILITY

A. SYSTEM M.B.T.F.

The system goal is 4000hrs
MTTR 2.0 hrs or less
MTTI 4.0 hrs or less

B. SUB-ASSEMBLY M.B.T.F.

ALL VALUES ARE

CALCULATED USEING

MIL SPEC STANDARD

217 @ G.B.

Calaulated MTBF UNIT	hrs X 1000	
MOTHERBOARD	15.1	
U.B.W.	91.9	
F.O.T/R	278.0	
B.B.A	92.53	
H7865	23.9	
MONITOR	15.5	
LK201	66.8	(less usease than the PC350)
CABLES	2000.0	
MOUSE	35.0	
TILT/SWIVEL	n/a	
FIBER CABLE	87.71	(300m,at min bend rad.)

Min bend radius = 3.0cm for whole cable
Min bend radius = 2.0cm for sub-channel (check the spec.)

11.0 MAINTAINABILITY

No customer maintainable components. No customer adjustable controls

12.0 HUMAN FACTORS

FLOW CHART OF INTERFACE -- TO BE SUPPLIED

13.0 REFERENCE MATERIAL

DEC. STD. 158 UNIBUS SPECIFICATION

A-PS-17-00333-0-0 CABLE,FIBER OPTIC,TWO CHANNEL,UNTERMINATED

A-PS-17-00343-0-0 CABLE,FIBER OPTIC,TWO CHANNEL,TERMINATED

A-SP-H7865-0-0 POWER SUPPLY, H7865,MULTIPLE OUTPUT,5V,+12V,-12V

A-PS-30-20240-0-0 MONITOR,ALPHA/GRAPHIC VIDEO, 19 INCH, MONOCHROME

A-PS-30-20037-0-0 TABLET, DIGITIZING

A-PS-30-20038-0-1 MOUSE,,HAND HELD

A-SP-LK201-A-2 LK201 KEYBOARD DESIGN SPECIFICATION

WORKSTATION GRAHPIC ARCHITECTURE V1.0, 1 MARCH 1983, H LEVY

Driver spec --- latest copy april 82

firmware spec --- not available

uCode spec

Diag spec level 2b